WHAT IS CLAIMED IS:

1. An SRAM memory cell comprising:

first and second inverters interconnected between first and second data nodes, each inverter comprising complementary MOS transistors connected in series between a DC voltage reference and a ground reference, and

means for programming the MOS transistors adapted for causing, after programming, an irreversible degradation of a gate oxide layer of some at least of the transistors.

2. The SRAM memory cell according to Claim 1, wherein each inverter comprises a first PMOS transistor and a second NMOS transistor coupled in series between the voltage reference and the ground reference, the data nodes (N1, N2) being formed respectively between the two NMOS and PMOS transistors of the inverters.

3. The SRAM memory cell according to Claim 1 wherein the degradable MOS transistor is a thin gate oxide layer transistor.

4. The SRAM memory cell according to Claim 3, wherein the oxide layer is degradable at least locally in such a way as to obtain, during the reading of the cell, a variation in the current delivered by the transistor.

5. The SRAM memory cell according to Claim 1, wherein the programming means comprise, for each inverter, a programming transistor (28, 30) or a diode linked between a programming control line (PROG) and one of the transistors of the inverter.

6. The SRAM memory cell according to Claim 5, wherein the programming means comprise one of an NMOS transistor or a programming diode that selectively links the gate of the degradable transistor to a programming voltage reference delivering a voltage level able to cause, jointly with the DC voltage supply source linked to the drain of the degradable transistor, a degradation in the gate oxide layer of the transistor, the programming transistor being driven by the programming control line.

7. The SRAM memory cell according to Claim 1, further comprising means for causing the cell to operate as an SRAM memory after programming.

8. The SRAM memory cell according to Claim 7, wherein the inverters are interconnected by way of NMOS transistors linked to a control line for instructing the cell to operate as an SRAM memory.

9. The SRAM memory cell according to Claim 8, wherein a drain electrode and source electrode of each of the said NMOS transistors are respectively linked to the gate of the transistors of one of the inverters.

10. An SRAM memory cell of the 6T type which includes a pair of load transistors connected to a reference voltage, the memory cell further including a programming circuit coupled to a gate of at least one of the load transistors, the programming circuit delivering a voltage to the gate of the at least one load transistor which is sufficient to cause an irreversible gate oxide degradation for purposes of programming the memory cell to permanently store a certain data value.

11. The SRAM memory cell of claim 10 wherein the programming circuit comprises a programming transistor having a source/drain terminal connected to a gate of the at least one load transistor and a drain source terminal connected to a voltage reference.

12. The SRAM memory cell of claim 10 wherein the programming circuit comprises:

a first programming transistor having a source/drain terminal connected to a gate of a first one of the load transistors and a source/drain terminal connected to a voltage reference; and

a second programming transistor having a drain/source terminal connected to a gate of a second one of the load transistors and a source/drain terminal connected to the voltage reference.

13. The SRAM memory cell of claim 12 wherein the first and second programming transistors are connected in series with each other.

14. An SRAM memory cell of the 6T type including a pair of inverter transistors which are cross-coupled and a pair of load transistors, the memory cell further including a operational configuration circuit that selectively connects and disconnects a gate of a first load transistor to a gate of a first inverter transistor and selectively connects and disconnects a gate of a second load transistor to a gate of a second inverter transistor.

15. The SRAM memory cell of claim 14 wherein operational configuration circuit comprises a pair of control transistors whose gates are connected to receive a control signal, a first control transistor having its source terminal connected to a gate terminal of a first load transistor and its drain terminal connected to a gate terminal of a first inverter transistor, and a second control transistor having its drain terminal connected to a gate terminal of a second load transistor and its source terminal connected to a gate terminal of a second inverter transistor.

16. The SRAM memory cell of claim 14, further comprising a programming circuit coupled to the gate of at least one of the load transistors, the programming circuit delivering a voltage to the gate of the at least one load transistor which is sufficient to cause an irreversible gate oxide degradation for purposes of programming the memory cell to permanently store a certain data value.

17. The SRAM memory cell of claim 16 wherein the programming circuit comprises a programming transistor having a source/drain terminal connected to a gate of the at least one load transistor and a drain source terminal connected to a voltage reference.

18. The SRAM memory cell of claim 10 wherein the programming circuit comprises:

a first programming transistor having a source/drain terminal connected to a gate of a first one of the load transistors and a source/drain terminal connected to a voltage reference; and

a second programming transistor having a drain/source terminal connected to a gate of a second one of the load transistors and a source/drain terminal connected to the voltage reference.

19. A method for operating an SRAM memory cell of the 6T type, comprising:

delivering a voltage to a gate of at least one load transistor in the SRAM memory cells which is sufficient to cause an irreversible gate oxide degradation for purposes of programming the memory cell to permanently store a certain data value.

20. The method of claim 19 further comprising selectively connecting and disconnecting the gate of each load transistor to a gate of its series connected inverter transistor in the SRAM memory cell.